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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,144	08/27/2004	Douglas D. Coolbaugh	BUR920040107US1	5143

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
01/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,144	COOLBAUGH ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-9 and 11-20* is/are pending in the application.

4a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9 and 11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on October 31st, 2007 has been entered. A new rejection is made as set forth in this Office Action. Claims (1-3, 5-9 and 11-20) are pending in the application, in which claims 15-20 are withdrawn from consideration.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-9 and 11-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Gau (U.S. Patent 6,949,440).

In re claim 1, **Gau** discloses a varactor structure comprising: a semiconductor substrate **40** of a first conductivity type, the substrate **40** including a subcollector **42** of a second conductivity type (col. 4, lines 11-30) located below an upper region of the substrate **40**, the first conductivity type is different from the

second conductivity type; a well region located in the upper region of the substrate **40**, wherein the well region includes outer well regions **44/52** of the second conductivity type and an inner well region **46** of the first conductivity type, each well of alternating conductivity type of the well region is separated at an upper surface by an isolation region **50** (col. 4, lines 31-40 and FIG. 11) and

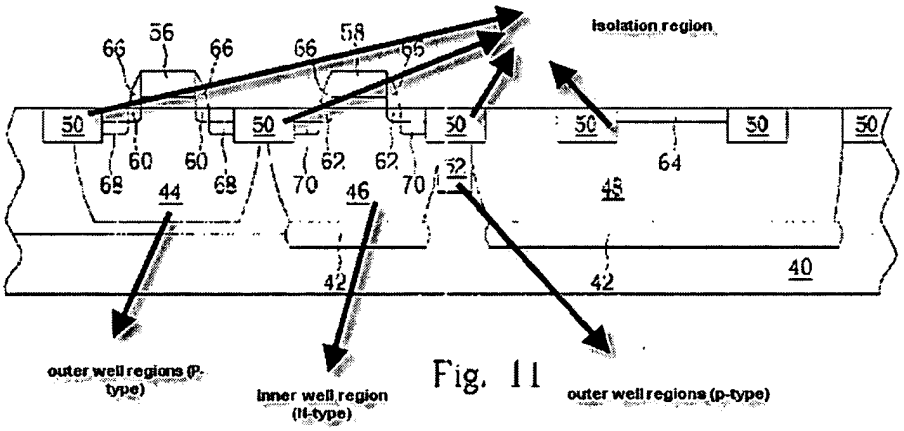

Fig. 11

each outer well region has an upper surface which includes a source/drain region **60/62** (col. 4, lines 57-67); a field effect transistor having at least a gate conductor **58** of the first conductivity type located above the inner well region **46**; and wherein the outer well regions **44/52** and the inner well region 46 are in contact with the subcollector **42** (col. 4, line 67 to col. 5, line 6 and FIG. 11).

In re claim 2, as applied to claim 1 above, **Gau** discloses all claimed limitations including the limitation wherein the first conductivity type comprises a p-type dopant and second conductivity type comprises a n-type dopant (col. 4, lines 11-30).

In re claim 3, as applied to claim 1 above, **Gau** discloses all claimed limitations including the limitation wherein the first conductivity type comprises a n-type dopant and the second conductivity type comprises a p-type dopant (col. 4, lines 11-30).

In re claim 5, as applied to claim 1 above, **Gau** discloses all claimed limitations including the limitation wherein each inner well region **46** and each outer well region **44/52** extends beneath the isolation region **50** to the subcollector **42** such that neighboring inner and outer well regions **44/52** are in contact with each other along the entire depth of each well region beneath the isolation region (FIG. 11).

In re claim 6, as applied to claim 1 above, **Gau** discloses all claimed limitations including the limitation wherein the upper region of the substrate **40** comprises an epitaxial semiconductor layer (col. 3, lines 25-44).

In re claim 7, as applied to claim 1 above, **Gau** discloses all claimed limitations including the limitation wherein the field effect transistor further comprises a gate dielectric located beneath the gate conductor **58**, a hard mask located on the gate conductor, at least one spacer **66** located on sidewalls of the gate conductor **58** and abutting source/drain regions **62** (col. 4, line 67 to col. 5, line 5 and FIG. 11).

In re claim 8, as applied to claim 1 above, **Gau** discloses all claimed limitations including the limitation wherein the gate conductor **58** comprises polysilicon (col. 3, lines 35-38).

In re claim 9, **Gau** discloses a varactor structure comprising a p-type semiconductor substrate **40**, the p-type substrate including an n-type subcollector **42** located below an upper region (col. 4, lines 11-30) of the substrate **40**; a well region located in the upper region of the substrate **40**, wherein the well region includes outer N-well regions **46/48** and an inner P-well region **52**, each well of alternating conductivity type of the well region is separated at an upper surface by an isolation region **50** (col. 4, lines 31-40 and FIG. 11) and

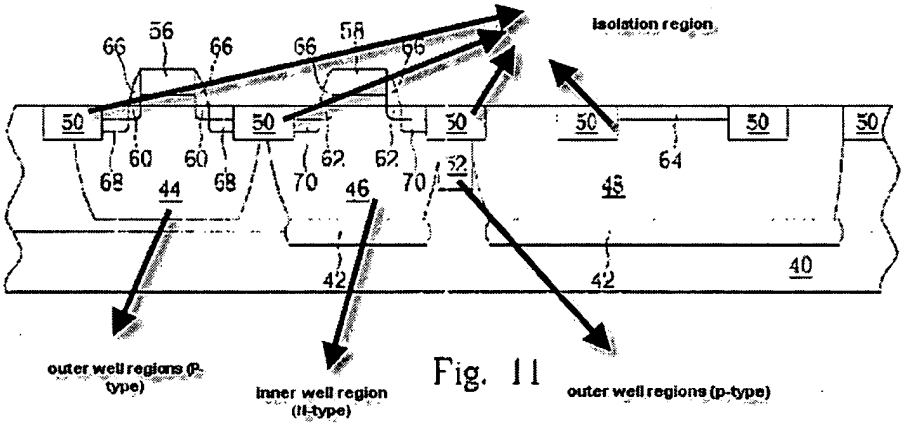

Fig. 11

each outer well region has an upper surface which includes a source/drain region **60/62** (col. 4, lines 57-67); a field effect transistor having at least a p-type gate conductor 58 located above the inner P-well region; and wherein the outer N-well regions **46/48** and the inner P-well region **52** are in contact with the subcollector (col. 4, line 67 to col. 5, line 6 and FIG. 11).

In re claim 11, as applied to claim 9 above, **Gau** discloses all claimed limitations including the limitation wherein each outer N-well region **46/48** and each inner P-well region **52** extends beneath the isolation region **50** to the

subcollector such that neighboring outer **46/48** and inner well regions **52** are in contact with each other along the entire depth of each well region beneath the isolation region (FIG. 11).

In re claim 12, as applied to claim 9 above, **Gau** discloses all claimed limitations including the limitation wherein the upper region of the substrate **40** comprises an epitaxial semiconductor layer (col. 3, lines 25-44).

In re claim 13, as applied to claim 9 above, **Gau** discloses all claimed limitations including the limitation wherein field effect transistor further comprises a gate dielectric located beneath the gate conductor **58**, a hard mask located on the gate conductor **58**, at least one spacer **66** located on sidewalls of the gate conductor **58** and abutting source/drain regions **62** (col. 4, line 67 to col. 5, line 5 and FIG. 11).

In re claim 14, as applied to claim 9 above, **Gau** discloses all claimed limitations including the limitation wherein the gate conductor comprises polysilicon (col. 3, lines 35-38).

Response to Applicants' Amendment and Arguments

4. Applicants' arguments filed October 31st, 2007 have been fully considered but they are not persuasive.

Applicants contend that the reference Gau (U.S. Patent 6,949,440), herein known as Gau, fails to disclose, inter alia, wherein the outer well regions and the inner well region are in contact with the subcollector.

In response to Applicants' contention that Gau does not teach or suggest wherein the outer well regions and the inner well region are in contact with the subcollector, Examiner respectfully disagrees.

Applicants' attention is respectfully directed to (col. 4, line 67 to col. 5, line 6 and FIG. 11) where Gau discloses that the outer well regions 44/52 and the inner well region 46 are in contact with the subcollector 42. Since the Applicants' claimed invention, as currently amended, does not clearly specify if the outer well regions 44/52 and the inner well region 46 are electrically or physically contact the subcollector. It is respectfully submitted that the outer well regions 44/52 and the inner well region 46 are capable of electrically contacting the subcollector region 42.

For this reason, Examiner holds the rejection proper.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

K.N.

Brook Kebede

BROOK KEBEDE
PRIMARY EXAMINER